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(54) ADDITION OPERATING DEVICE AND SEMICONDUCTOR MEMORY DEVICE WITH ADDITION OPERATION FUNCTION

(57)Abstract:
PROBLEM TO BE SOLVED: To provide an addition operation by utilizing a memory array itself.
SOLUTION: When an addition operation of each digit is to be performed about two pieces of binary data, the value of a binary input bit is preliminarily written in each memory cell MCa, MCb and MCc according to a normal writing procedure in a DRAM. After a bit line pair BLi and BLi- are precharged to reference voltage 0.5 VDD, each corresponding word line Wa, Wb and Wc is made active and the respective storage charge of the cell MCa, MCb and MCc are added up through a common bit line BLi. A 1st sense amplifier S/A1 performs a normal binary type detection amplification operation and outputs the binary data of '1' or '0' in accordance with the level relation between the potential Ve4 of the line BLi and comparison reference voltage Vref1. A

2nd sense amplifier S/A2 also performs a normal binary type detection amplification operation and outputs the binary data of '1' or '0' in accordance with the level relation between the potential Ve4 of the line BLi and comparison reference voltage Vref2. As a result, 2-bit binary data (Ve4 (MSB) and Ve4 (LSB)) are obtained by means of the amplifiers S/A1 and S/A2.

CLAIMS

[Claim(s)]
[Claim 1]An add operation device comprising:
A binary data feeding means which gives binary data of 1 bit which has any one value in a binary set up beforehand.
The 1st conversion method changed into value data which has any one value in a value which adds said N binary data given from said binary data feeding means, and is beforehand set up in the total (N+1) (N+1).
The 2nd conversion method that detects a value of the aforementioned (N+1) value data generated by said adding means, and changes the detected value into binary data of the number of predetermined bits.

[Claim 2]The add operation device according to claim 1 which at least one in said N binary data added is carry data, it considers a least significant bit in binary data of said binary number obtained from said 2nd conversion method as a peace output, and considers a high order bit of the remaining all as an output of a carry.
[Claim 3]An add operation device comprising:
Binary parameter supply elements which give the 1st 1-bit electrical parameter that has any one value in a quantization level binary set up beforehand.
The 1st conversion method changed into the 2nd electrical parameter that has any one value in a quantization level value (N+1) which adds said 1st N electrical

parameter (N is two or more integers) given from said binary parameter supply elements, and is beforehand set up in the total.
The 2nd conversion method that detects a value of said 2nd electrical parameter generated by said adding means, and changes the detected value into binary data of the number of predetermined bits.

[Claim 4]A semiconductor memory device with an add operation function characterized by comprising the following.
Two or more memory cells which are connected to one of bit lines and accumulate an electric charge of a quantization level binary corresponding to binary data by 1 bitwise.
A sense amplifier connected to each complementary bit line pair.
An adding means which generates bit line potential of a quantization level value (N+1) which adds an electric charge accumulated in N selected memory cells (N is two or more integers), respectively on 1 or two or more common bit lines, and has a pressure value corresponding to total of these charge quantity on said bit line.
A bit line potential supply means which gives said bit line potential separately via said bit line respectively corresponding to said sense amplifier of the number equal to the number of bits required for a binary numeral of N, A comparison reference voltage feeding means which gives different comparison reference voltage with which it was beforehand set for detecting said bit line voltage as said two or more sense amplifiers, respectively, A sense amplifier control means which obtains binary data which makes said two or more sense amplifiers detect said bit line potential based on said comparison reference voltage which each corresponds to predetermined timing, respectively, and expresses an aggregate value with them combining each binary output of these sense amplifiers.

[Claim 5]Said adding means precedes adding an electric charge accumulated in said N selected memory cells, respectively, The semiconductor memory device with an add operation function according to claim 4 containing a precharge means for precharging said common 1 or two or more bit lines to a predetermined reference potential.
[Claim 6]Said adding means precedes adding an electric charge accumulated in said N selected memory cells, respectively, The semiconductor memory device with an add operation function according to claim 4 including a stored charge copy means which copies each stored charge to another predetermined memory cell about a part or all of said N memory cells, respectively.
[Claim 7]Said adding means precedes adding an electric charge accumulated in said N selected memory cells, respectively, The semiconductor memory device with an add operation function according to claim 4 including a reversal copy means which carries out logic inversion of the electric charge accumulated in said a part of N memory cells, and is copied to another predetermined memory cell.

[Claim 8]The semiconductor memory device with an add operation function according to claim 4 which is accumulating an electric charge as which at least one in said N selected memory cells expresses carry data.
[Claim 9]The sum of an electric charge by which said adding means is accumulated in said N selected memory cells, respectively, The semiconductor memory device with an add operation function according to any one of claims 4 to 8 which generates bit line potential of a value according to each capacitance and parasitic capacitance of said common 1 or two or more bit lines.
[Claim 10]The semiconductor memory device with an add operation function according to claim 4 with which said bit line potential supply means contains a transistor connected between each bit line of two or more of said sense amplifiers which adjoin each other.
[Claim 11]The semiconductor memory device with an add operation function according to claim 4 to which said sense amplifier control means shifts predetermined time to said two or more sense amplifiers at order from the higher one of a beam of a binary output which constitutes binary data of said binary number, and sensing operation is made to perform.
[Claim 12]The semiconductor memory device with an add operation function according to claim 11 with which said comparison reference voltage feeding means determines standard-for-comparison potential to said sense amplifier of a beam of the one low rank according to a binary output obtained from said sense amplifier of a beam of each higher rank.
[Claim 13]A semiconductor memory device with an add operation function characterized by comprising the following.
Two or more memory cells which are connected to one of bit lines and accumulate an electric charge of a quantization level binary corresponding to binary data by 1 bitwise.
An adding means which generates bit line potential of a quantization level value (N+1) which adds an electric charge accumulated in N selected memory cells (N is two or more integers), respectively on one common bit line, and has a pressure value corresponding to total of these charge quantity on said bit line.
M sense amplifiers connected in parallel with each complementary bit line pair (M is the number of bits required for a binary numeral of N).
A bit line potential supply means which gives said bit line potential separately to said M sense amplifiers via said bit line, A comparison reference voltage feeding means which gives different comparison reference voltage with which it was beforehand set for detecting said bit line voltage as said M sense amplifiers, respectively, A sense amplifier control means which obtains binary data of M bit which makes said M sense amplifiers detect said bit line potential based on said comparison reference voltage which each corresponds to predetermined timing, respectively, and expresses an aggregate value with them combining each binary output of these sense amplifiers.

DETAILED DESCRIPTION

[Detailed Description of the Invention]

[0010]

[Field of the Invention]This invention relates to the semiconductor memory device which is applied to the device which performs an add operation about the data of a binary number, especially can perform not only memory of information but data processing of addition.

[0020]

[Description of the Prior Art]The principle of the add operation to binary data is shown in drawing 40. If the number of bits of the augend a and the addend b is carried out, respectively (n+1), the single figure add operation of a time (n+1) will be performed at a time in all sequentially from a least significant bit (a0, b0). In the add operation of each beam (x beam), three input bits, the augend bit ax, the addend bit bx, and the carry bit cix from a low order digit, are applied by equivalent weighting, and the sum Sx and the carry bit Cox to a high-order digit are generated according to a truth value table like a graphic display.

[0030]The circuitry of the add operation circuit which realizes faithfully logic of the Boolean algebra showing the above-mentioned truth value table and this Boolean algebra in a gate circuit is shown in drawing 41. Although the conventional binary add operation device makes the gate number less than the thing of a graphic display, it comprises same logic circuit fundamentally.

[0040]

[Problem(s) to be Solved by the Invention]The above conventional logic circuit type add operation devices have a limit in respect of processing time or efficiency to large-scale data. the case where necessary add operation processing is performed by image processing etc. -- every 1 pixel -- or repeat execution of the add operation of every one line must be carried out, and the concurrency of the add operation cannot be carried out about all the image data of one frame. Therefore, on the whole, considerable calculation time is needed. With the composition which carries out parallel arrangement, circuit structure enlarges the add operation circuit for one line.

[0050]The purpose of this invention is to provide the add operation device which makes an instantaneous add operation possible to large-scale data.

[0060]Another purpose of this invention is to provide the semiconductor memory device with an add operation function which realizes an add operation using the memory array itself.

[0070]Other purposes of this invention are to provide the semiconductor memory

device with an add operation function which it not only can perform data storage which is an original function of a dynamic RAM to usual, but realizes the add operation of data with the composition which added few circuit elements.

[0080]

[Means for Solving the Problem]In order to attain the above-mentioned purpose, an add operation device of this invention is provided with the following.

A binary data feeding means which gives binary data of 1 bit which has any one value in a binary set up beforehand.

The 1st conversion method changed into value data which has any one value in a value which adds said N binary data given from said binary data feeding means, and is beforehand set up in the total (N+1) (N+1).

The 2nd conversion method that detects a value of the aforementioned (N+1) value data generated by said adding means, and changes the detected value into binary data of the number of predetermined bits.

[0090]Another add operation device of this invention is provided with the following.

Binary parameter supply elements which give the 1st 1-bit electrical parameter that has any one value in a quantization level binary set up beforehand.

The 1st conversion method changed into the 2nd electrical parameter that has any one value in a quantization level value (N+1) which adds said 1st N electrical parameter (N is two or more integers) given from said binary parameter supply elements, and is beforehand set up in the total.

The 2nd conversion method that detects a value of said 2nd electrical parameter generated by said adding means, and changes the detected value into binary data of the number of predetermined bits.

[0100]A semiconductor memory device with an add operation function of this invention is provided with the following.

Two or more memory cells which are connected to one of bit lines and accumulate an electric charge of a quantization level binary corresponding to binary data by 1 bitwise.

A sense amplifier connected to each complementary bit line pair.

An adding means which generates bit line potential of a quantization level value (N+1) which adds an electric charge accumulated in N selected memory cells (N is two or more integers), respectively on 1 or two or more common bit lines, and has a pressure value corresponding to total of these electric charges on said bit line.

A bit line potential supply means which gives said bit line potential separately via said bit line respectively corresponding to said sense amplifier of the number equal to the number of bits required for a binary numeral of N, A comparison reference voltage feeding means which gives different comparison reference voltage with which it was beforehand set for detecting said bit line voltage as said two or more sense amplifiers,

respectively, A sense amplifier control means which obtains binary data which makes said two or more sense amplifiers detect said bit line potential based on said comparison reference voltage which each corresponds to predetermined timing, respectively, and expresses an aggregate value with them combining each binary output of these sense amplifiers.

[0110]In the above-mentioned semiconductor memory device, preferably, Said adding means may contain a precharge means for precharging said common 1 or two or more bit lines to a predetermined reference potential, before adding an electric charge accumulated in said N selected memory cells, respectively.

[0120]Said adding means precedes preferably adding an electric charge accumulated in said N selected memory cells, respectively, A stored charge copy means which copies each stored charge to another predetermined memory cell about a part or all of said N memory cells, respectively may be included.

[0130]Said adding means may also include preferably a reversal copy means which carries out logic inversion of the electric charge accumulated in said a part of N memory cells before adding an electric charge accumulated in said N selected memory cells, respectively, and is copied to another predetermined memory cell.

[0140]At least one in said N selected memory cells may be accumulating an electric charge showing carry data preferably.

[0150]It may be the composition that said adding means generates preferably bit line potential of a value according to the sum of an electric charge accumulated in said N selected memory cells, respectively, each capacitance, and parasitic capacitance of said common 1 or two or more bit lines.

[0160]Said bit line potential supply means may be the composition containing a transistor connected between each bit line of two or more of said sense amplifiers which adjoin each other preferably.

[0170]It may be the composition of said sense amplifier control means shifting predetermined time to said two or more sense amplifiers at order from the higher one of a beam of a binary output which constitutes binary data of said binary number, and making sensing operation performing preferably.

[0180]A comparison reference voltage feeding means may be the composition of determining standard-for-comparison potential to said sense amplifier of a beam of the one low rank according to a binary output obtained from said sense amplifier of a beam of each higher rank, preferably.

[0190]Another semiconductor memory device with an add operation function of this invention is provided with the following.

Two or more memory cells which are connected to one of bit lines and accumulate an electric charge of a quantization level binary corresponding to binary data by 1 bitwise.

An adding means which generates bit line potential of a quantization level value (N+1)

which adds an electric charge accumulated in N selected memory cells (N is two or more integers), respectively on one common bit line, and has a pressure value corresponding to total of these charge quantity on said bit line.
M sense amplifiers connected in parallel with each complementary bit line pair (M is the number of bits required for a binary numeral of N).
A bit line potential supply means which gives said bit line potential separately to said M sense amplifiers via said bit line, A comparison reference voltage feeding means which gives different comparison reference voltage with which it was beforehand set for detecting said bit line voltage as said M sense amplifiers, respectively, A sense amplifier control means which obtains binary data of M bit which makes said M sense amplifiers detect said bit line potential based on said comparison reference voltage which each corresponds to predetermined timing, respectively, and expresses an aggregate value with them combining each binary output of these sense amplifiers.

[0200]
[Embodiment of the Invention]Hereafter, the example of this invention is described with reference to drawing 1 – drawing 39.
[0210]First, the basic principle of this invention is explained per drawing 1 – drawing 5. For example, if the add operation to the two bit binary number (n+1) data a (an .... a1 a0) and b (bn .... b1 b0) is taken for an example, as this invention shows to drawing 1, The mean value e4x of the number of 4 ** or four values is introduced between the input bit (ax, bx, cix) of each beam, and an outputted bit (cox, sx). This mean value e4x expresses with the number of 4 ** the value obtained by adding three input bits (ax, bx, cix) by equal weighting.
[0220]If each input bit (ax, bx, cix) is regarded as the value (0/1) on the number of 4 ** instead of the value (0/1) of a binary number and is added as the 1st step **, the mean value e4x of the number of 4 ** will be acquired.
[0230]Next, the mean value e4x of the above-mentioned number of 4 ** is changed into 2-bit binary data [e4x (MSB), e4x (LSB)] as the 2nd step. Here, the high order bit e4x (MSB) of the lower bit e4x (LSB) of this binary data corresponds with the sum sx of the beam (x) concerned in accordance with the carry cox to a high-order digit (x+1). That is, the same result of an operation as the usual full adder is obtained.
[0240]The example of basic constitution of the add operation device which realizes the above-mentioned algorithm of this invention is shown in drawing 2.
[0250]Like a graphic display, while electrically connecting the three capacitors Ca, Cb, and Cc with equal capacitance to common lead DL via the switch SW, for example, a transistor switch, respectively, the end of lead DL is connected to the 4 value detection type voltage detector 10. The predetermined electric charge Q is beforehand stored in each capacitors Ca, Cb, and Cc, or it is made to hardly store an electric charge. It is equivalent to this writing in 1 of binary data, or 0, and the voltage

Va of each capacitors Ca, Cb, and Cc, Vb, and Vc take the value of either a predetermined charge-voltages value (for example, 3 volts) or a non-charge-voltages value (for example, 0 volt).

[0260]If all the switches SW are closed all at once, the electric charge accumulated, respectively will be added to each capacitors Ca, Cb, and Cc via lead DL. Potential Ve4 on lead DL will become a pressure value decided by total Qt of these stored charge, and capacitance of each capacitors Ca, Cb, and Cc, if the parasitic capacitance of lead DL is disregarded. Since capacitance is constant and there are four kinds (0Q, 2Q, 3Q) of total Qt of stored charge on a quantization level or a discrete level, Potential Ve4 on lead DL takes the value of a value (referred to as Ve4 (0)) in case Qt is 0, a value (referred to as Ve4 (1)) in case Qt is Q, a value (referred to as Ve4 (2)) in case Qt is 2Q, or a value (referred to as Ve4 (3)) in case Qt is 3Q.

[0270]The voltage detector 10 should just detect or distinguish to any of 4 value level (Ve4 (0), Ve4 (1), Ve4 (2), Ve4 (3)) potential Ve4 on this lead DL corresponds. Only the capacity Q predetermined in a fluid is contained in each, or this structure all vacates also with it the three containers Ka into which it hardly goes, Kb, and Kc for the graduated cylinder 12 to which 4 value graduations were attached, and is similar to reading the graduation of the graduated cylinder 12.

[0280]And the voltage detector 10 should just output the detection result with 2-bit binary data [Ve4 (MSB) and Ve4 (LSB)]. Namely, Ve4 (0) When it detects, [0, 0] are outputted, and it is Ve4 (1). When it detects, [0, 1] are outputted, when Ve4 (2) are detected, [1, 0] are outputted, and it is Ve4 (3). What is necessary is just to output [1, 1], when it detects. High-order-bit Ve 4 (MSB) of this 2-bit binary data is equivalent to the carry cox to a high-order digit (x+1), and lower bit Ve 4 (LSB) is equivalent to the sum sx of the beam (x) concerned.

[0290]Another example of basic constitution of the add operation device by this invention is shown in drawing 3. This method connects three current path Pa selectable to any one in a predetermined quantization level binary (this example R1, R2), Pb, and Pc for each resistance in parallel to the power supply voltage Vcc, He is trying for the 4 value detection type current detecting circuit 16 to detect all the current Ie4 which the current Ia which flows into each current path circuits Pa, Pb, and Pc when the main switch SWM is closed, Ib, and Ic added, and were put together using the suitable current sensor 14. Here, it is the resistance R1. Let resistance be a thing large about 1000 times, more for example than the resistance of the resistance R0.

[0300]The configuration switch SWa formed in each current path circuits Pa, Pb, and Pc, SWb, and SWc are switched to the left of a figure, or a right position according to the value (0/1) of a binary number, According to the switching position, each current Ia, Ib, and Ic take any one value in a predetermined quantization level binary (referred to as I0 and I1). Therefore, composite current Ie4 takes any one value in four

quantization level values [3I0, (2I0+I1), (I0+2I1), 3I1].

[0310]The current detecting circuit 16 detects any in four values [3I0, (2I0+I1), (I0+2I1), 3I1] composite current Ie4 is, and should just output the 2-bit binary data [Ie4 (MSB) and Ie4 (LSB)] showing the detection result.

[0320]Thus, it is possible to use various electrical parameters with the add operation device of this invention.

[0330]The following examples explain the application which applied this invention to the dynamic RAM (DRAM).

[0340]First, the basic principle in the case of realizing this invention by DRAM is explained about drawing 4 and drawing 5.

[0350]Within DRAM, each memory cell MC which consists of one transistor and one capacitor cell (capacitor) is electrically connected to one of the bit lines BLi, The bit line BLi is it, complementary bit line BLi-, and a pair, shifts, and is connected to that sense amplifier S/A. In each memory cell MC, a transistor constitutes a switch and a capacitor cell accumulates an electric charge.

[0360]Therefore, as shown in drawing 4, the composition electrically connected to sense amplifier S/A via the bit line BLi with common three memory cells MCa, MCb, and MCc can be obtained. Here, if sense amplifier S/A is constituted from a 4 value detection type sense amplifier, the thing equivalent to the above-mentioned add operation device of drawing 2 will be obtained. but in DRAM, rather than capacitance Cs of memory cell MC, it is markedly alike, and since it is large, the parasitic capacitance CB of the bit line BL also needs to apply this parasitic capacitance CB to one of the circuit elements.

[0370]Like the usual data storage in DRAM, when writing data "1" in each memory cell MCa, MCb, and MCc, the electric charge Q of the specified quantity is stored up, and when writing in data "0", it is made not to store up most electric charges. If it sees with a voltage level, the fixed charge voltages VDD (for example, 3 volts) correspond to data "1", and non-charge voltages (for example, 0 volt) correspond to data "0."

[0380]As mentioned above, when performing the add operation of each beam about two binary data a and b, the value of the binary input bit (ax, bx, cix) is beforehand written in each memory cell MCa, MCb, and MCc by the usual write-in procedure in DRAM.

[0390]And after precharging the bit line pair BLi and BLi- to 0.5VDD (VDD is power supply voltage) which is the usual reference voltage, the word line Wa which each corresponds, Wb, and Wc are activated, The stored charge of each memory cell MCa, MCb, and MCc is added via the common bit lines BLi. Four kinds of pressure values Ve4 (0) as which potential Ve4 of the bit line BLi is expressed in a following formula (1), (2), (3), and (4) according to the truth value table of drawing 4 when it does so Ve4 (1) Ve4 (2) Ve4 (3) Any one inner value is taken.

[0400]

Ve4 (0) =0.5VDD {1−3Cs /(CB+3Cs)} .... (1)

Ve4 (1) =0.5VDD {1− Cs/(CB+3Cs)} .... (2)

Ve4 (2) =0.5VDD {1+Cs/(CB+3Cs)} .... (3)

Ve4 (3) =0.5VDD {1+3Cs /(CB+3Cs)} .... (4)

[0410]Upper type (1) − (4) to 0<Ve4 (0) Ve4 (1) <0.5VDD and 0.5 VDD<Ve4 (2) Ve4 (3) There is size relation of <VDD, It is 0<Ve4 (0) in more detail. <0.5VDD {1−2Cs /(CB+3Cs)} <Ve4 (1) <0.5VDDD <Ve4 (2) <0.5VDD {1+2Cs /(CB+3Cs)} <Ve4 (3) It turns out that there is size relation of <VDD.

[0420]Then, what combined binary detection type sense amplifier S/A1 of a couple and S/A2 as 4 value detection type sense amplifier S/A in this example as shown, for example in drawing 5 is adopted.

[0430]0.5VDD is given to 1st sense amplifier S/A1 as comparison reference voltage Vref1 from the complementary bit line BLi− side. Sense amplifier S/A1 performs usual binary type detection amplifying operation, and it outputs the binary data of "1" or "0" according to the size relation of potential Ve4 of the bit line BLi, and comparison reference voltage Vref1. More, (VDD, 0) are outputted to details on BLi and BLi− at the time of Ve4>0.5VDD, and (0, VDD) are outputted on BLi and BLi− at the time of Ve4<0.5VDD.

[0440]On the other hand to 2nd sense amplifier S/A2, as comparison reference voltage Vref2 from the complementary bit line BLi− side, When the detection result of sense amplifier S/A1 of the above 1st is "1", 0.5VDD {1+2Cs /(CB+3Cs)} is given, and when the detection result of S/A1 is "0", 0.5VDD {1−2Cs /(CB+3Cs)} is given.

[0450]This sense amplifier S/A2 performs usual binary type detection amplifying operation, and it outputs the binary data of "1" or "0" according to the size relation of potential Ve4 of the bit line BLi, and comparison reference voltage Vref2. In details, it is on BLi and BLi− () more at the time of Ve4> {1+2Cs /(CB+3Cs)} or Ve4> {1−2Cs /(CB+3Cs)}. [VDD and] 0) is outputted and (0, VDD) are outputted on BLi and BLi− at the time of Ve4< {1+2Cs /(CB+3Cs)} or Ve4< {1−2Cs /(CB+3Cs)}.

[0460]As a result, it is Ve4 (0) from sense amplifier S/A1 and S/A2. When detected, (0, 0), Ve4 (1) When detected, it is (0, 1), and Ve4 (2). When detected, it is (1, 0), and Ve4 (3). When detected, the 2−bit binary data [Ve4 (MSB) and Ve4 (LSB)] of (1, 1) is obtained.

[0470]Like the above, high−order−bit Ve 4 (MSB) of this 2−bit binary data can be made into the carry cox to a high−order digit (x+1), and the lower bit V4e (LSB) can be made into the sum sx of the beam (x) concerned.

[0480]Next, the composition and the operation of the example of DRAM with an add operation function by this example are explained about drawing 6 − drawing 15.

[0490]The circuitry of the important section of DRAM with an add operation function in this example is shown in drawing 6. In this DRAM, base elements, such as memory

cell MC in a memory cell array and an array, word line W, the bit line BLi, BLi-, and sense amplifier S/A, are the usual composition. In order to flow through / intercept each sense amplifier S/A and a memory array selectively, each bit line BLi and the transfer gate (T16, T17, T26, T27) provided on BLi- are also conventional means.

[0500]Characteristic composition, Sense amplifier S/A1 of a ****** couple, and S/A2. Temporary memory cell MC01 for add operations to between memory cell arrays (the example of drawing 6 inside of the transfer gate T16, T17, T26, and T27), MC02, MC11, MC12, MC13, MC21, MC22, MC23. And it is that the transistor T03, T04, T14, T15, T24, and T25 are added.

[0510]Two temporary memory cell MC12 and MC13 are connected more to details in parallel between bit line BL1 and ground potential. The transistor T14 is connected between the node of the transistor T13 of MC13, and the capacitor C13, and ground potential.

[0520]Two temporary memory cell MC11 and MC01 are connected between bit line BL2 and ground potential. The transistor T03 is connected between the node of the transistor T01 of MC01, and the capacitor C01, and bit line BL1-. The transistor T15 is connected between bit line BL1 and BL2.

[0530]Two temporary memory cell MC22 and MC23 are connected in parallel between bit line BL1- and ground potential. The transistor T24 is connected between the node of the transistor T23 of MC23, and the capacitor C23, and ground potential.

[0540]Two temporary memory cell MC21 and MC02 are connected in parallel between bit line BL2- and ground potential. The transistor T04 is connected between the node of the transistor T02 of MC02, and the capacitor C02, and bit line BL1. The transistor T25 is connected between bit line BL2 and BL2-.

[0550]The necessary control signal phi is given to each transistor T from the sequence control section 20 (drawing 9). In detail, it is bit line BL1 and BL2. phi 1 is given to the upper transfer gate T17 and T16. phi 2 is given to the transistor T15. phi 3 is given to each transistor T11 of temporary memory cell MC11 and MC12, and T12. phi 4 is given to the transistor T13 of temporary memory cell MC13. phi 5 is given to the transistor T14. phi 6 is given to the transistor T01 of temporary memory cell MC01. phi 7 is given to the transistor T03.

[0560]phi 8 is given to the transistor T04. phi 9 is given to the transistor T02 of temporary memory cell MC02. phi 10 is given to the transistor T24. phi 11 is given to the transistor T23 of temporary memory cell MC23. phi 12 is given to each transistor T21 of temporary memory cell MC21 and MC22, and T22. phi 13 is given to the transistor T25. phi 14 is given to the transfer gate T26 and T27.

[0570]Command CD1 for data writing/read-out more nearly usual than a memory control logic section (not shown) etc. in the sequence control section 20, Command CD2 for the add operation in this example, etc. is inputted, and also from a clock circuit (not shown), clock CK is inputted and the various above-mentioned control

signals phi are generated to a predetermined sequence and timing.

[0580]The circuitry of sense amplifier S/A (S/A1, S/A2) is shown in drawing 7. This sense amplifier S/A will be in an active state by control signal phiA of the complementary couple from the sequence control section 20, and phiA-, The complementary bit line pair BL, BL - The upper potential is inputted and it is constituted as a binary detection type differential amplifier which detects the difference and even the level of the power supply voltage VDD and the level of ground potential amplify.

[0590]Although not illustrated in drawing 6, the precharge circuit 22 of circuitry as shown, for example in drawing 8 is established in the outside of the memory cell array near each sense amplifier S/A. The precharge electric supply line 24 is connected to the precharge power supply circuit which is not illustrated.

[0600]If the sequence control section 20 activates control signal phiP on H level, precharge-transistors TP1, TP2, and equalizing transistor TP3 will flow, respectively, The bit line pair BLi and BLi- are precharged at the voltage level (0.5VDD) of precharge reference voltage VP from a precharge power supply circuit.

[0610]In drawing 6, each sense amplifier S/Ai is alternatively chosen by Y address selection signal YSi from Y address decoder (not shown). Selection will connect BLi-, the input and output BLi, i.e., the bit line pair, of the sense amplifier S/Ai concerned, to data input/output line I/O and I/O-.

[0620]Next, in this DRAM, the operation in the case of carrying out the add operation of the two bit binary number (n+1) data A (An....A one A0) and B (An .... A1 A0) as shown in drawing 10 is explained. In drawing 11 referred to by the following explanation - drawing 21, Y address selection line YS and data input/output line I/O, and I/O- is excluded for facilitating of an illustration.

[0630]It precedes performing an add operation first and both binary data A which is the target of an add operation, and B are stored in suitable memory cell MC in a memory cell array by the usual write mode in DRAM.

[0640]for example, it is shown in drawing 11 -- as -- The bit Bn of the addend data B .... B1 B0 -- bit line BL1 -- storing in a side -- The bit An of the augend data A .... A1 A0 -- bit line BL2 -- it stores in a side. It is important to write the bit of the same beam in both the data A and B in memory cell MC on the same word line W here. In usual DRAM operation like this data storage processing, the control signal phi 2 for add operations - phi13 are fixed to the inactive state (L level).

[0650]The step of the beginning of an add operation is shown in drawing 12. Addition is begun from the least significant bit A0 and B0.

[0660]First, choose the least significant bit A0 and the word line W0 by which common connection is carried out to the two memory cells MC and MC in the memory cell array which stores B0, respectively, and by the usual DRAM read-out procedure. Sensing of these least significant bits A0 and the contents of B0 is carried out to

sense amplifier S/A1 and S/A2 via bit line BL1 and BL2. In this case, use the control signal phi 1 and phi 14 as H level, it is made to flow through each transfer gate T16, T17, T26, and T27, and a memory cell array, and sense amplifier S/A1 and S/A2 are electrically connected.

[0670]When the sensing operation of sense amplifier S/A1 and S/A2 is completed, the control signal phi 3 is activated on H level, and the least significant bit A0 and the contents of B0 are written in temporary memory cell MC11 and MC12, respectively. It means that the least significant bit A0 and the contents of B0 were copied to temporary memory cell MC11 and MC12 from the memory cells MC and MC in a memory cell array by this, respectively.

[0680]When this copy operation is completed, the control signal phi 3 is returned to L level, temporary memory cell MC11 and MC12 are electrically intercepted from bit line BL1 and BL2, respectively, and the contents of a copy are made to save. Operation of both sense amplifier S/A1 and S/A2 is stopped, and the word line W0 is returned to L level. It means that the information on a copied material (A0, B0) was re-written in now also within the memory cell array.

[0690]On the other hand, use the control signal phi 5 as H level, it is made to flow through the transistor T14, and "0" of binary data is written in temporary memory cell MC13. This binary data "0" is used for the input carry of a least significant digit operation.

[0700]After the above-mentioned copy operation activates the precharge circuit 22 of drawing 8, and precharges each bit line pair (BL1 and BL1-) and (BL2 and BL2-) to reference voltage 0.5VDD.

[0710]Next, as shown in drawing 13, the control signal phi 12 is activated on H level under the state of precharge, and precharge reference voltage 0.5VDD is written in temporary memory cell MC21 and MC22. Make the control signal phi 2 and phi 13 activation (H level), and it is made to flow through the transistor T15 and T25 immediately after that, and is bit line BL1 and BL2. Comrades and BL1-, and BL2- are connected by a short condition, respectively.

[0720]The control signal phi 1 and phi 14 are returned to L level, and the transfer gate T16, T17, T26, and T27 are made into the OFF state just before the end of precharge. Thereby, in future operation operations, a memory cell array is electrically separated from sense amplifier S/A.

[0730]After the end of the above-mentioned precharge, the control signal phi 3 and phi 4 are activated on H level. This state is intelligibly shown in drawing 14 as an electric network. This is equivalent or equivalent to the electric network of drawing 4. Therefore, the same truth value table as drawing 4 and formula (1) - (4) are applied, and it is bit line BL1 and BL2. Upwards, the potential Vdata which has the same quantization level value as potential Ve4 of drawing 4 is obtained. At this time, sense amplifier S/A1 has not been activated yet.

[0740]Next, as shown in drawing 15, the control signal phi 2 and phi 13 are returned to L level, the transistor T15 and T25 are made into an OFF state, and it is bit line BL1 and BL2. Comrades and BL1−, and BL2− are separated electrically, respectively. Since each bit line BL is placed by the high impedance state also after this separation, that potential is not changed. Namely, bit line BL1 and BL2 The upper potential Vdata maintains the same pressure value as before, and the potential on bit line BL1− and BL2− maintains reference voltage (0.5VDD).
[0750]Here, sense amplifier S/A1 is activated. Sense amplifier S/A1 is bit line BL1. The voltage difference between the upper potential Vdata and the reference voltage (0.5VDD) on complementary bit line BL1− is detected and amplified. Namely, it is bit line BL1 at the time of Vdata>0.5VDD (at that is, the time of Vdata (2) or Vdata (3)). The voltage of a VDD level is outputted upwards and the voltage of ground potential VGND is outputted on bit line BL1−. It is bit line BL1 at the time of Vdata<0.5VDD (at that is, the time of Vdata (0) or Vdata (1)). The voltage of ground potential VGND is outputted upwards and the voltage of a VDD level is outputted on bit line BL1−.
[0760]The electric network of the circumference of sense amplifier S/A1 at the time of performing the above sensing operation is shown in drawing 16. It is bit line BL1 by the sensing operation of this sense amplifier S/A1 so that I may be understood. The binary voltage (VDD/VGND) obtained upwards expresses the carry output Co of the least significant bit A0 and the add operation result of B0.
[0770]Thus, even if sense amplifier S/A1 operates, the potential on bit line BL2 and BL2− maintains the pressure value Vdata till then and 0.5VDD, respectively, without being influenced by what.
[0780]Activate the control signal phi 7 and phi 8 on H level before and after the sensing operation of sense amplifier S/A1, it is made to flow through the transistor T03 and T04, respectively, and the sensing information on sense amplifier S/A1 is written in temporary memory cell MC01 and MC02.
[0790]That is, sense amplifier S/A1 is Vdata (2) at bit line BL1 up. Or Vdata (3) When it detects and VDD and VGND are outputted on bit line BL1 and BL1−, respectively, While the voltage VGND on bit line BL1− is written in temporary memory cell MC01, it is bit line BL1 to temporary memory cell MC02. The upper voltage VDD (carry output Co = ″1″) is written in.
[0800]Sense amplifier S/A1 is Vdata (0) at bit line BL1 up. Or Vdata (1) When it detects and VGND and VDD are outputted on bit line BL1 and BL1−, respectively, While the voltage VDD on bit line BL1− is written in temporary memory cell MC01, it is bit line BL1 to temporary memory cell MC02. The upper voltage VGND (carry output Co = ″0″) is written in.
[0810]But in this example, only MC02 which copies the carry output Co functions effectively among both temporary memory cell MC01 and MC02, and MC01 does not function substantially.

[0820]Since the control signal phi 3 and phi 4 are maintaining the active state (H level), it is bit line BL1 also to temporary memory cell MC12 and MC13. The binary voltage (VDD/VGND) of the upper carry output Co is copied. It is MC13 for carry storing that this copy has a meaning. The data copied to MC12 will be replaced with other information in next operation. Sense amplifier S/A2 has not been activated yet at this time.
[0830]If the copy of the carry output Co (VDD/VGND) of temporary memory cell MC02 is completed as mentioned above, as shown in drawing 17, the control signal phi 7 and phi 8 will be returned to L level, and the transistor T03 and T04 will be intercepted.
[0840]Subsequently, the control signal phi 9 is activated on H level, and the electric charge accumulated in both temporary memory cell MC02 and MC21 on bit line BL2-, respectively is added.
[0850]The state at this time is intelligibly shown in drawing 18 as an electric network. bit line BL2 which is one difference input of sense amplifier S/A1 -- the upper potential Vdata -- the pressure value (0), i.e., Vdata, at the time - Vdata (3) Either is maintained. [state / of drawing 14] However, potential Vref2 on bit line BL2- which is a difference input of another side shifts to the pressure value expressed with the following formula (5) or either of (6) according to the carry output Co (VDD/VGND) stored in temporary memory cell MC02.
[0860]That is, when the carry output Co is 1 (VDD), it is Vref2=0.5VDD {1+2Cs /(CB+3Cs)}.... (5)
[0870]the time of the carry output Co being 0 (VGND) -- Vref2=0.5VDD {1-2Cs /(CB+3Cs)} -- -- (6)
[0880]Derivation of these formulas (5) and (6) is shown in drawing 19. The capacitor cell C02 of temporary memory cell MC02 connected to bit line BL2- of a reference voltage supply circuit and MC21 and the capacitance of C21 are chosen as the predetermined value for obtaining the above-mentioned reference voltage Vref2. In this example, it is C02=Cs, C21=Cs / 2, for example.
[0890]In drawing 17, sense amplifier S/A2 is again activated immediately after activating the control signal phi 9 as mentioned above.
[0900]When the carry output Co is 1 (VDD), sense amplifier S/A2 is bit line BL2. The voltage difference between the upper potential Vdata (Vdata (2) or Vdata (3)) and the reference voltage Vref2 on complementary bit line BL2- (5) is detected and amplified.
[0910]Namely, it is bit line BL2 at the time (at that is, the time of Vdata (3)) of Vdata>Vref2 (5). The voltage VDD is outputted upwards and the voltage VGND is outputted on bit line BL2-. The voltage VGND is outputted on the bit line BL2 at the time (at that is, the time of Vdata (2)) of Vdata<Vref2 (5), and it outputs the voltage VDD on bit line BL2-.
[0920]When the carry output Co is 0 (VGND), sense amplifier S/A2 is bit line BL2. The

voltage difference between the upper potential Vdata (Vdata (0) or Vdata (1)) and the reference voltage Vref2 on complementary bit line BL2- (6) is detected and amplified.
[0930]Namely, it is bit line BL2 at the time (at that is, the time of Vdata (1)) of Vdata>Vref2 (6). The voltage VDD is outputted upwards and the voltage VGND is outputted on bit line BL2-. The voltage VGND is outputted on the bit line BL2 at the time (at that is, the time of Vdata (0)) of Vdata<Vref2 (6), and it outputs the voltage VDD on bit line BL2-.
[0940]In this way, the binary voltage (VDD/VGND) obtained on the bit line BL2 by the sensing operation of sense amplifier S/A2 expresses the sum S0 of the least significant bit A0 and the add operation result of B0. Bit line BL1 The upper potential is maintaining the binary voltage (VDD/VGND) showing the carry output C0 of the least significant bit A0 and the add operation result of B0.
[0950]As a result, the result of the add operation to the least significant bit A0 and B0 is binary data (Co, So) (it carries out and obtained by both sense amplifier S/A1, S/A2, or both bit line pair B (BL1 and BL1-) and (BL2 and BL2-).).
[0960]Next, the binary data (Co, So) of an add operation result is stored in the suitable place in a memory cell array. For example, as shown in drawing 20, the control signal phi 1, phi 14, and the word line WO may be activated, and it may store in the least significant bit A0 for addition, and memory cell MC in which B0 was stored by overwrite. You may write in another memory cell MC to save the original data A0 and B0. It is also possible to read data (Co, So) to the memory exterior via data input/output line I/O and I/O-.
[0970]The add operation processing to the least significant bit A0 and B0 is ended above. Next, the 2nd bit (the 2nd figure) A1 and the processing same about B1 as the above are repeated from the lowest.
[0980]That is, in the first step, the bit A1 of the arithmetic object stored in the memory cells MC and MC of relevance in a memory cell array by the same procedure as the above and the contents of B1 are copied to temporary memory cell MC11 and MC12, respectively.
[0990]However, as shown in drawing 21, the control signal phi 5 is fixed to L level (deactivation level). By this, the carry output Co stored in temporary memory cell MC13 by the previous (low order digit) add operation is used for the carry input C1 by this add operation. Next processing is performed by the same sequence as the time of the add operation of the above-mentioned least significant bit.
[1000]The above-mentioned operation explained the procedure of having once written the data for addition in a memory cell array, and performing an add operation.
[1010]However, it is also possible to perform an add operation simultaneously with the writing of data. In this case, at the same time as it activates word line W of relevance within a memory cell array, the control signal phi 3 is also activated and the data written in in a memory cell array is written also in temporary memory cell MC11 and

MC12. In the add operation of a least significant bit, the control signal phi 5 is activated on H level like the above, and the data "0" of temporary memory cell MC13 is written in.

[1020]And after completion of the writing of the data to a memory cell array, the control signal phi 1 and phi 14 are returned to L level, the transfer gate T16, T17, T26, and T27 are intercepted, and a memory array is separated from an add operation part. What is necessary is after that, just to perform add operation processing by the same sequence as the above.

[1030]Next, the example which enabled it to perform not only an add operation but subtraction operation in this DRAM is described.

[1040]The subtraction in a binary number computes the two's complement value of a subtrahend, and is attained by adding the two's complement value of a minuend and a subtrahend.

[1050]The two's complement of a binary number carries out logic inversion of all the bits of the binary number, and is obtained by adding 1 to the value generated by the reversal operation. For example, in order to obtain a two's complement with a binary number [01011010] of 8 bits, all the bits are reversed first. A binary number [10100101] is obtained by this operation. The numbers [10100110] produced by adding 1 to this number are an original number of two's complement values.

[1060]The composition of the important section of DRAM by this example is shown in drawing 22. In this example, the independent control signal phi 31, phi 32, phi 121, and phi 122 are respectively given to temporary memory cell MC11, MC12, MC21, and MC22. Not ground potential but the control signal phi 15 is given to the transistor T14 and the terminal of another side of T24 which are connected to temporary memory cell MC13 and MC23. Other portions are the same composition as the above-mentioned add operation circuit.

[1070]But in this example, it does not matter as composition which chooses both temporary memory cell MC11 and MC12 with the same control signal phi. Since the control signal phi 121 and phi 122 are controlled only by the same timing, they are actually good also as the same control signal phi. It dared to be referred to as the separate control signal phi 121 and phi 122 because the composition which makes it correspond to the separate control signal phi 31 and phi 32 mutually in the opposite hand of a sense amplifier, and is easy to realize object nature of the layout of a sense amplifier portion is provided.

[1080]Also in subtraction operation, data (A, B) required for an operation is beforehand written in the suitable place in a memory cell array by the write mode of the usual DRAM. In that case, phi 2, phi 31, phi 32, phi 4, phi 5, phi 6, phi 7, phi 8, phi 9, phi 10, phi 11, phi 121, phi 122, phi 13, and 15 are maintained at a non-active state (L level) among the control signals phi, Since it will be set to the usual DRAM if phi1 and phi14 are activated on H level and it is made to flow through the transfer gate T16,

T17, T26, and T27, data is written in in the state.

[1090]In the step of the beginning of subtraction operation, the least significant bit A0 of a minuend (this example A) is copied to temporary memory cell MC11. It can come, simultaneously the least significant bit of the two's complement of a subtrahend (B) is generated.

[1100]A solid line shows the element and control signal which are activated at this step to drawing 23. First, activate the word line W0 and the least significant bit A0 of the minuend A and the subtrahend B and B0 are read to sense amplifier S/A1 and S/A2 via bit line BL1 and BL2, respectively, Sensing of the binary data A0 and B0 is carried out to both sense amplifier S/A1 and S/A2. Then, the control signal phi 31, phi 7, and phi 8 are activated on H level. The control signal phi 5, phi 10, and phi 15 are activated on H level simultaneously with it.

[1110]But phi 8 and phi 10 may be maintained at L level. In this example, in order to balance the control signal phi 7 and phi 15 in consideration of the object nature of a control signal to a sense amplifier, respectively, phi 8 and phi 10 are activated.

[1120]The least significant bit A0 of the minuend A stored in the memory cell array is copied to temporary memory cell MC11 via sense amplifier S/A2 by the above-mentioned operation. On the other hand, the least significant bit B0 of the subtrahend B is read to sense amplifier S/A1, and value B0- which was obtained on bit line BL1- and by which bit flipping was carried out is written in temporary memory cell MC01.

[1130]Bit line BL1 This value is not used although the data of B0 read upwards is written in temporary memory cell MC02. Therefore, it is not necessary to perform this writing.

[1140]Data "1" is written in temporary memory cell MC13 by both the control signal phi 5 and phi 15 being set to H level as mentioned above. Therefore, the sum of two data, temporary memory cell MC01 and MC13, is a least significant bit of the two's complement of the subtrahend B. It means that preparation of the least significant bit required for subtraction was completed now.

[1150]Next, the control signal phi 1 and phi 14 are returned to L level, and a memory cell array is separated from an add operation circuit. And after returning the control signal phi 31, phi 7, and phi 8 to L level, bit line pair (BL1 and BL1-), (BL2 and BL2-), and sense amplifier S/A1 and S/A2 are precharged to 0.5VDD. The control signal phi 5 and phi 10 are returned to L level by the start of the subtraction operation following the next.

[1160]Next, the subtraction operation of a least significant bit is started. That is, the least significant bit A0 of the minuend A and the least significant bit of the two's complement of the subtrahend B are added. Operation of a series of this add operation is shown in drawing 24, drawing 25, drawing 26, and drawing 27. Since the add operation principle and the operating procedure are the same as the

above-mentioned add operation, detailed explanation is omitted.

[1170]The subtraction to the next (the 2nd figure) bit of a least significant bit is fundamentally the same as the operation of a least significant bit. However, when generating the two's complement of a subtrahend, in the least significant bit, the data of "1" was written in temporary memory cell MC13, but since it is not necessary to add "1" except a least significant bit, operation of writing "1" data in temporary memory cell MC13 is not performed.

[1180]The carry information Co and the peace (sum) information So on a binary are acquired from both sense amplifier S/A1 and S/A2 like the above-mentioned example as a result of the add operation of the least significant bit A0 of the minuend A, and the least significant bit of the two's complement of the subtrahend B. The carry information Co is needed by the subtraction operation of the following high order bit. As shown in drawing 28, temporary memory cell MC13 can be used for being convenient as a momentary holding element of the carry information Co like the time of the add operation of the above-mentioned example.

[1190]In this example, although parallel operation to the bit depth direction of data is not performed, data can be gathered, it can incorporate into DRAM and the above 1-bit addition (subtraction) operations can be simultaneously performed about all the data in DRAM. For example, if there are 4000 sets of sense amplifiers (S/A1, S/A2) in DRAM, 4000 1-bit all addition (subtraction) operations can be performed at once.

[1200]Such package data processing is advantageous to performing filtering, interpolation processing, motion detection processing, etc. to the image data for one frame, for example in image processing.

[1210]In the above-mentioned example, the add operation part is provided inside the transfer gate T16, T17, T26, and T27. These transfer gates are theoretically unnecessary. However, at the time of an add operation, these transfer gates can be made into an OFF state, and the bit line in a memory cell array can be electrically separated from an add operation part. Since the length of the significant part of bit line BL1 used by an add operation, BL1, -, BL2, and BL2- is shortened by this and bit line volume load (parasitic capacitance CB) can be made small, while operation operation can be performed at high speed, there is an advantage that power consumption which charge of volume load takes can be lessened.

[1220]The sense amplifier which constitutes an add operation part is constituted from sense amplifier S/A1 of a ****** couple, and S/A2 by the above-mentioned example in the usual DRAM. For this reason, it faces adding an add operation function, is not necessary to increase the circuit area of a sense amplifier section, and is efficient also in respect of operation also at the point of a design and manufacture.

[1230]As described above, it faces storing data (A, B) required for an operation in a memory cell array, and the bit of the same beam can be written in the memory cell connected to the same word line W. And the same word line W can be chosen, those

bits can be read simultaneously, and it can copy to predetermined temporary memory cell MC of an add operation part simultaneously via both sense amplifier S/A1 and S/A2.

[1240]It is possible to exclude MC11, MC12, MC13, MC21, MC22, and MC23 among temporary memory cell MCs of add operation circles in the above-mentioned example, and to make those functions substitute for the memory cell in a memory cell array.

[1250]Although the area of a sense amplifier section will double as compared with the usual DRAM, as shown, for example in drawing 29, the composition which assigns the 4 value detection type sense amplifier (S/A1, S/A2) by this example to one bit line pair (BLi and BLi-) is also possible.

[1260]Also in the composition of drawing 29, it is possible to exclude MC11, MC12, MC13, MC21, MC22, and MC23 among temporary memory cell MCs of an add operation part, and to make the memory cell in a memory cell array substitute for those functions.

[1270]In the composition corresponding to [in the sense amplifier (S/A1, S/A2) of 4 value detection type in this way] one bit line pair (BLi and BLi-) at 1 to 1, The bit of binary data A of an augend (minuend) and the bit of binary data B of an addend (subtrahend) are stored in the memory cell on the same bit line within a memory cell array, At the time of an add operation, the stored charge of three memory cell MCs will be added on the same bit line BLi like drawing 5.

[1280]Below, the address assigning method of the data in DRAM of this method is explained about drawing 30 - drawing 34. In order to explain explanation briefly, both the augend data A and the addend data B are made into triplet width, and suppose that it is it the data constellation which stood in a row eight pieces respectively.

[1290]Arrangement of each data bit stored in the memory before the add operation is shown in drawing 30. Here, in A (b, t), b shows a bit position (0, 1, 2, and a number are attached toward the high order bit from the lower bit.), and t shows the ranking in the inside of a data constellation. B (b, t) is also the same. C (x, t) is used in order to store the carry information on an add operation temporarily.

[1300]Although X decoder 30 chooses one word line (line) usually specified by row address information (activation), it is constituted in the add operation mode of this example so that it may mention later, and three word lines (line) can be chosen simultaneously (activation). The Y decoder 32 functions as connecting to a data input/output line one sense amplifier S/A(i) specified for column address information. Sense amplifier S/A(i) of each sequence contains sense amplifier S/A1 of a couple which was described above, and S/A2.

[1310]As described above, it performs 1 bit of add operations at a time for every 1 memory operation cycle one by one from a least significant bit. 1 memory operation cycle is fundamentally [as the 1 bit read-out cycle of the usual DRAM] the same.

[1320]A (b, t) and B (b, t) are beforehand written in in the memory cell array by the

write mode of the usual DRAM like the above-mentioned example. All C (x, t) is set to "0."

[1330]First, a least significant bit is added by the 1st memory operation cycle. For this reason, as shown in drawing 31, least significant bit A (0, t), B (0, t), and three lines of the carry bit C (x, t) are chosen simultaneously, and an add operation which was described above is performed. And the peace information So acquired as a result of this operation is set to A (0, t) and/or B (0, t), and write back of the carry information Co is carried out to C (x, t), respectively.

[1340]In the 2nd memory operation cycle, as shown in drawing 32, three lines of the 2nd bits A (1, t) and B (1, t) and the carry bit C (0, t) are simultaneously chosen from the lowest, and the same add operation as the above is performed. And the peace information S1 acquired by the operation is set to A (1, t) and/or B (1, t), and write back of the carry information C1 is carried out to C (0, t), respectively.

[1350]In the 3rd memory operation cycle, an add operation which chooses simultaneously three lines of the 3rd bits (top) (2, t) A (2, t) and B and the carry bit C (1, t), and described them above as shown in drawing 33 is performed. And the peace information S2 acquired by the operation is set to A (2, t) and/or B (2, t), and write back of the carry information C2 is carried out to C (1, t), respectively.

[1360]Therefore, as shown in drawing 34, the data (S2 S1S0+C2) of a final add operation result is stored in each applicable position in a memory array. These result-of-an-operation data can be read by the Read mode in the usual DRAM.

[1370]In this method, two or more words (line) must be chosen as mentioned above in the case of an add operation. The word (referred to as Wc) which stores the carry information C must be chosen in all the cycles. Both timing must be shifted when carrying out write back of the carry information C and the peace information S after the result of an operation.

[1380]Therefore, what is necessary is just to provide the control circuit for controlling ON and OFF of the word line Wc for carry independently of other word line W. The circuit which makes two word lines selectable only at the time of operation operation already has many examples.

[1390]One of the easiest examples is shown in drawing 35. This method carries out multiplex [of the control signal SEL] to the least significant bit X0 of X address signal inputted into an X decoder, and X0-. X decoder 30' operates as a usual decoder which specifies one word line, when SEL is "0", and when SEL is "1", it operates as a decoder which makes simultaneous selection of the two continuous word lines. The control signal Carry for choosing the word line Wc for carry C is given separately.

[1400]In the above-mentioned example, 4 value processing (binary ->4 value -> binary) performs the add operation of binary data (0/1).

[1410]However, the principle of this invention is not limited to 4 value processing, is possible also for octal processing (binary ->4 value -> binary) and

sexadecimal-of-hexadecimal processing (a binary -> sexadecimal of hexadecimal -> binary), or can also realize decimal-or-denary processing (a binary -> decimal or denary -> binary), for example so that I may be understood from the above-mentioned explanation. In this invention, the add operation of a binary is an execution target and four values, an octal, etc. are only treated as a value in the case of the intermediate treatment of an add operation.

[1420]Below, octal processing is explained. In a numerical expression, the dignity of each beam is a exponentiation of 2. Therefore, when the numerical value "7" of a single figure is acquired as the result of an operation, for example on the occasion of octal number processing, if this is changed into a binary number, it will be set to "111" and will become a numerical value of triple figures. When it sees as add operation operation of a binary number, "1" at the right end of "111" shows the number of the beams, it is shown that "1" of middle has beam going up to the following high-order digit, and it is shown that "1" of a left end has beam going up to the high-order digit of 2 beyond.

[1430]As an example, there are the numerical value V, W, and X of a binary number, Y, and Z, and suppose that it is V= 10, W= 11, X= 01, Y= 01, and Z= 11.

[1440]The add operation of these five numbers shall be calculated via octal processing, and the result of the number of binaries (binary number) shall be obtained. First, it is as follows when it asks for the sum of five given numbers of the minimum beams.

V (LSB)+W (LSB)+X(LSB)+Y(LSB)+Z (LSB) =0+1+1+1+1 =4(octal number)=100 (binary number) .... (7)

[1450]It is as follows, when the carry from a low order digit is disregarded and it asks for the sum of the following beam.

V(2^{nd}LSB) +W(2^{nd}LSB) +X (2^{nd} (LSB)+Y (2^{nd} (LSB)+Z (2^{nd} (LSB) =1+1+0+0+1=3(octal number)=011 (binary number) .... (8))))

[1460]The least significant digit of the add operation result of these [from the result of the above-mentioned formula (7)] five figures is "0" in a binary numeral. Since there is no carry from the result of the above-mentioned formula (7) to the following high-order digit, a right end numerical value "1" brings a result of the above-mentioned formula (8) to the 2nd low order digit of an add operation result, and it is set to "1" by a binary numeral.

[1470]Since the left end value is "1", the result of the above-mentioned formula (7) has a carry to the following high-order digit (that is, the 3rd low order digit). If these are taken into consideration, the 3rd and 4th low order digit of an add operation result will be set to "0" and "1", respectively.

[1480]Therefore, the added result obtained eventually is "1010" in a binary numeral.

[1490]As mentioned above, if an octal (octal number) is used by add operation processing so that I may be understood, carry propagation will amount to figures, a

following high-order digit and the following (2 beyond) high-order digit, double [top]. In the case of sexadecimal of hexadecimal, carry propagation amounts to figures triple [top].

[1500]When octal processing is adopted by the intermediate treatment of an operation by the add operation of binary data, simultaneous addition of a maximum of five coded data can be performed.

[1510]Since each coded data is given with a binary number, a single beam takes either value of "0" and "1." For example, all the possible minimums are [in / by the add operation of eight coded data / each beam] the decimal numerals 0 in the case of "0", and all the possible maximums are the decimal numerals 8 in the case of "1." If a mean value (1-7) is also included, 9 value state can be taken. Since it is most efficient to control by octal processing in the octal state, simultaneous operation is good to consider it as seven coded data. And for a certain reason, simultaneous operation will be performed in five coded data inputs and two carry information inputs after all that carry information spreads from a double figures low rank as described above.

[1520]Simultaneous operation in the case of sexadecimal of hexadecimal is performed in 12 coded data inputs and three carry information inputs so that I may be understood easily.

[1530]The algorithm which carries out simultaneous addition of the five coded data in a triplet or octal processing of triple figures is shown in drawing 36. a1, a2, a3, a4, and a5 are five coded data inputs. $co2_0$ of a least significant digit is a carry signal to the following high-order digit, and $co1_1$ is a carry signal to the following next high-order digit. Although $co1_3$ of the 3rd figure does not consider it as the signal to the following next high-order digit but it is considered as the signal to the following beam, if weighting (x2) is carried out at the time of the input of the following beam, it will use becoming homonymy mathematically.

[1540]The algorithm of the add operation at the time of applying the same weighting as the above to all the beams is shown in drawing 37.

[1550]The example of an octal detection type sense amplifier circuit is shown in drawing 38. In this example, the cell for copying the data in a memory cell array among temporary memory cells, or holding carry information temporarily is omitted. Tolan FAGETO T13 of a graphic display, T14, T15, T23, T24, and T25 are omissible. In the following explanation, the control signal phi 1 and phi 12 are fixed to the active state (H level).

[1560]The this octal detection type sense amplifier circuit comprises sense amplifier S/Aof three ****** 1, S/A2, and S/A3 in the usual DRAM.

[1570]Operation is fundamentally [as 4 value detection type of the above-mentioned example] the same. The electric charge of the quantization level binary respectively corresponding to seven binary data is read from seven memory cells in a memory cell array (not shown) on bit line BL1, BL2, and BL3 (also including carry information). In

that case, the control signal phi 2 and phi 3 are beforehand used as H level, and the transistor T12 and T11 are made into switch-on.
[1580]By this, Potential Vb8 (0) of the quantization level octal beforehand set as the difference input terminal [on the other hand / (left-hand side)] of each sense amplifier S/A1, S/A2, and S/A3 via each bit line BL1, BL2, and BL3 -Vb8 (7) Inner any one potential Vb8 is transmitted equally.
[1590]At this time, 0.5VDD which is predetermined reference voltage is given to the difference input terminal of another side (left-hand side) of each sense amplifier S/A1, S/A2, and S/A3. The control signal phi 10 and phi 11 are beforehand used as H level, and, of course, make the transistor T21 and T22 switch-on. The control signal phi 6 and phi 7 are activated on H level, respectively, and the control signal phi 4, phi 5, phi 8, and phi 9 are used as L level, respectively.
[1600]Next, after using phi3 and phi10 as L level, respectively, sense amplifier S/A1 is activated, and it is bit line BL1. It is detected whether octal potential Vb8 [upper] is higher than 0.5VDD or low. That is, MSB (carry bit to a double figure high-order digit) is detected.
[1610]Bit line pair BL1 and BL1- is complementarily driven by the sensing operation of sense amplifier S/A1 even to the level of VDD and ground potential VGND. At this time, it is bit line BL2 and BL3. The upper potential is maintained by the above-mentioned octal potential Vb8, respectively. The potential on each complementary bit line BL2- and BL3- is also maintained by the above-mentioned reference voltage 0.5VDD.
[1620]The binary data (VDD/VGND) acquired by the sensing operation of sense amplifier S/A1 is written in temporary memory cell MC02 via the transistor T04.
[1630]Next, if phi 8 is activated on H level, it will be adjusted to sense amplifier S/A2 and value Vref2 in which reference voltage Vref1 in S/A3 reflected the sensing result of sense amplifier S/A1. As shown in drawing 39, reference voltage Vref2 is the octal potential Vb8 (0). -Vb8 (7) It is a position (level) of 1/4 or 3/4. In order to obtain this reference voltage Vref2, the capacitance of the capacitor cell C02 of temporary memory cell MC02 is chosen as a predetermined value.
[1640]Then, after using phi2 and phi11 as L level, sense amplifier S/A2 is activated, and it is bit line BL2. It is made to detect whether potential Vb8 [upper] is higher than reference voltage Vref2 after this adjustment, or it is low. That is, 2nd MSB (carry bit to a single figure high-order digit) is detected.
[1650]Although bit line pair BL2 and BL2- is complementarily driven by the sensing operation of sense amplifier S/A2 even to the level of VDD and VGND also in this case, Bit line BL3 The upper potential is maintained by the above-mentioned octal potential Vb8, and the potential on bit line BL3- is maintained by the above-mentioned reference voltage (1/4, or 3/4 level of an octal).
[1660]The binary data (VDD/VGND) acquired by the sensing operation of sense

amplifier S/A2 is written in temporary memory cell MC06 via the transistor T08.

[1670]Next, if phi 9 is activated on H level, reference voltage Vref2 in sense amplifier S / A3 will be adjusted to value Vref3 reflecting the sensing result of sense amplifier S/A2. As shown in drawing 39, Vref3 is the octal potential Vb8 (0). -Vb8 (7) It is a position (level) of 1/8, 3/8, 5/8, or 7/8. In order to obtain this reference voltage Vref3, the capacitance of the capacitor cell C06 of temporary memory cell MC06 is chosen as a predetermined value.

[1680]Then, sense amplifier S / A3 is activated and it is bit line BL3. It is made to detect whether potential Vb8 [upper] is higher than reference voltage Vref3 after this adjustment, or it is low. LSB (peace information S) is obtained as a result of this sensing operation.

[1690]

[Effect of the Invention]As explained above, according to this invention, an instantaneous add operation can be performed to large-scale data. It is also possible to realize an add operation using the memory array itself and it not only can perform to usual data storage which is an original function of a dynamic RAM in that case, but the add operation of data is realizable with the composition which added few circuit elements.

DESCRIPTION OF DRAWINGS

[Brief Description of the Drawings]

[Drawing 1]It is a figure showing the basic principle of the add operation of the binary number in this invention.

[Drawing 2]It is a figure showing the example of basic constitution of the add operation device which realizes the add operation algorithm of this invention.

[Drawing 3]It is a figure showing another example of basic constitution of the add operation device of this invention.

[Drawing 4]It is a figure showing the basic principle in the case of realizing this invention by DRAM.

[Drawing 5]It is a figure showing the basic principle in the case of realizing this invention by DRAM.

[Drawing 6]It is a figure showing the circuitry of the important section of DRAM with an add operation function by one example of this invention.

[Drawing 7]It is a circuit diagram showing the example of composition of the sense amplifier in an example.

[Drawing 8]It is a circuit diagram showing the example of composition of the precharge circuit in an example.

[Drawing 9]It is a block diagram showing the example of composition of the sequence control circuit in an example.
[Drawing 10]It is a figure showing the algorithm of the add operation in an example.
[Drawing 11]It is a figure showing the single step of the add operation in DRAM of an example.
[Drawing 12]It is a figure showing the single step of the add operation in DRAM of an example.
[Drawing 13]It is a figure showing the single step of the add operation in DRAM of an example.
[Drawing 14]It is a figure showing the single step of the add operation in DRAM of an example.
[Drawing 15]It is a figure showing the single step of the add operation in DRAM of an example.
[Drawing 16]It is a figure showing the single step of the add operation in DRAM of an example in an equivalent electric network.
[Drawing 17]It is a figure showing the single step of the add operation in DRAM of an example.
[Drawing 18]It is a figure showing the single step of the add operation in DRAM of an example in an equivalent electric network.
[Drawing 19]It is a figure showing derivation of the reference voltage in an example.
[Drawing 20]It is a figure showing the single step of the add operation in DRAM of an example.
[Drawing 21]It is a figure showing the single step of the add operation in DRAM of an example.
[Drawing 22]It is a figure showing the composition of the important section of DRAM by another example.
[Drawing 23]It is a figure showing the single step of the subtraction operation in DRAM of an example.
[Drawing 24]It is a figure showing the single step of the subtraction operation in DRAM of an example.
[Drawing 25]It is a figure showing the single step of the subtraction operation in DRAM of an example.
[Drawing 26]It is a figure showing the single step of the subtraction operation in DRAM of an example.
[Drawing 27]It is a figure showing the single step of the subtraction operation in DRAM of an example.
[Drawing 28]It is a figure showing the single step of the subtraction operation in DRAM of an example.
[Drawing 29]It is a figure showing the composition of the important section of DRAM by another example.

[Drawing 30]It is a figure for explaining the method of assigning the data in the method of drawing 29.
[Drawing 31]It is a figure for explaining the method of assigning the data in the method of drawing 29.
[Drawing 32]It is a figure for explaining the method of assigning the data in the method of drawing 29.
[Drawing 33]It is a figure for explaining the method of assigning the data in the method of drawing 29.
[Drawing 34]It is a figure for explaining the method of assigning the data in the method of drawing 29.
[Drawing 35]It is a figure showing the example of composition of an usable X decoder to the method of drawing 29.
[Drawing 36]It is a figure showing the algorithm of octal processing of this invention.
[Drawing 37]It is a figure showing another algorithm of octal processing of this invention.
[Drawing 38]It is a figure showing the composition of the octal detection type sense amplifier circuit by the example of this invention.
[Drawing 39]It is a figure for explaining an operation of octal processing of this invention.
[Drawing 40]It is a figure showing the add operation method of the binary number in the former.
[Drawing 41]It is a figure showing the conventional add operation device.
[Description of Notations]
Ca, Cb, Cc capacitor
10 4 value detection type voltage detector
Pa, Pb, Pc current path circuit
16 4 value detection type current detecting circuit
S/A 4 value detection type sense amplifier
S/A1, S/A2, S / A3 binary detection type sense amplifier
BL1, BL1 – Complementary bit line pair
BL2, BL2 – Complementary bit line pair
BL3, BL3 – Complementary bit line pair
MC01 and MC02 Temporary memory cell
MC11, MC12, and MC13 Temporary memory cell
MC21, MC22, and MC23 Temporary memory cell
T03, T04, T14, T24, T15, and T25 Transistor
20 Sequence control section
22 Precharge circuit
30 X decoder
32 Y decoder